REMARKS/ARGUMENTS

In the Office action mailed March 31, 2008, claims 1, 2, 5, 7, 9-12, 14-18, 21, and 24-36 have been rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,614,796 to Black et al. ("Black"). Claim 36 has been rejected under 35 U.S.C. § 103(a) over Black in view of U.S. Patent No. 6,697,914 to Hospodor et al ("Hospodor"). The Examiner is thanked for attention to the application.

Claims 1, 9, 11, 15, 27, 28, 29, 32, and 33 have been amended. Claims 5, 12, 26, and 30 are now canceled. Claims 37-39 are new.

Claim 1 has been amended to specify, in part, "at least one controller configured to process at least one fibre channel primitive received on the at least one fibre channel input to generate, based on the at least one fibre channel primitive, a plurality of states comprising an indication of what is routed to the at least one fibre channel output and what is routed to the at least one device output; a first multiplexer configured to route, in accordance with the plurality of states, data from the at least one fibre channel input or a current fill word to the at least one device output; and a second multiplexer configured to route, in accordance with the plurality of states, data from the at least one fibre channel input, data from the at least one device input, or data from an arbitration generator to the at least one fibre channel output." Support for the amendment may be found, for example, at Fig. 4 and p. 13, line 27 through p. 14, line 18 of the application as filed.

In rejecting prior claim 1, the Office action points to Black at Figs. 3, 4, and 7, col. 1, lines 14-17, col. 13, lines 33-42, col. 14, lines 9-22, col. 15, lines 52-61, col. 27, lines 22-35, and col. 34, lines 31-49.

Black's FIG. 3 shows a block diagram of a switched FCAL architecture with four fibre channel loops each connected to a switch control circuit where each switch control circuit connects to a crossbar switch and a protocol bus. Black's FIG. 4 shows a block diagram of the architecture of a switch to couple a plurality of FCAL nets to provide spatial reuse. The switch

includes multiple learning half bridges, each connected to a different fibre channel net, a crossbar switch interconnecting the half bridges, and a protocol bus connecting the half bridges to a routing table and a scoreboard. Black's FIG. 7 is a block diagram of a switch chip circuit component of Black's FCAL switch system including three net ports with SERDESs, elastic buffers, and state machines with the state machines connected to each other and to a backplane via a port multiplexer.

Black, at col. 1, lines 14-17, states, "Fibre Channel networks are known loop configuration networks that have a plurality of known type nodes such as servers, printers, disk arrays etc. all connected together by the loop." At col. 13, lines 33-42, Black partially describes the FCAL architecture of its Fig. 3 including control circuits that transmit primitives and data, do bypass switching, locate destinations for OPN signals, and send control signals to a crossbar switch. At col. 14, lines 9-22, Black partially describes the fibre channel switch of its Fig. 4 including presence of a crossbar switch and a plurality of learning half bridges, each with an input and an output for coupling to a fibre channel link. At col. 15, lines 52-61, Black describes part of the FCAL protocol used for hold back flow control. At col. 27, lines 22-35, Black describes an FCAL switch slice forwarding RRDY primitives or frame data between a paired fibre channel input and output. At col. 34, lines 31-49, Black partially describes a switch chip for an FCAL switch system including a port multiplexer controlled by three port state machines, with data paths connected between state machines or between state machine and backplane.

Black does not appear to describe "at least one controller configured to process at least one fibre channel primitive received on the at least one fibre channel input to generate, based on the at least one fibre channel primitive, a plurality of states comprising an indication of what is routed to the at least one fibre channel output and what is routed to the at least one device output," "a first multiplexer configured to route, in accordance with the plurality of states, data from the at least one fibre channel input or a current fill word to the at least one device output," and "a second multiplexer configured to route, in accordance with the plurality of states, data from the at least one fibre channel input, data from the at least one device input, or data from an arbitration generator to the at least one fibre channel output," as specified in amended claim 1.

Accordingly, claim 1 is allowable, as are dependent claims 2, 7, and 37-39.

Claim 9 has been amended to specify "receiving, from the at least one disk, data comprising at least one fibre channel primitive; processing the at least one fibre channel primitives to determine a plurality of states indicative of whether to route data received from the fibre channel arbitrated loop to the at least one disk or to the fibre channel arbitrated loop; routing, in accordance with the state determination, the data received from the fibre channel arbitrated loop; routing, in accordance with the state determination, the data received from the at least one disk; routing, in accordance with the state determination, a current fill word to the at least one disk; and routing, in accordance with the state determination, data from an arbitration generator to the fibre channel arbitrated loop."

In rejecting prior claim 9, the Office action points to Black at col. 1, lines 14-17, col. 13, lines 33-42, col. 14, lines 44-52, and col. 15, lines 52-61.

Black, at col. 1, lines 14-17, describes fibre channel networks as known loop configuration networks connecting known type nodes. At col. 13, lines 33-42, Black partially describes an FCAL architecture including control circuits that transmit primitives and data, do bypass switching, locate destinations for OPN signals, and send control signals to a crossbar switch. At col. 14, lines 44-52, Black describes a scoreboard and routing table in an FCAL switch with the scoreboard and routing table either shared or replicated for every port circuit and routing a request for a connection on a protocol bus when an OPN primitive arrives. At col. 15, lines 52-61, Black describes use of FCAL protocol OPN and RRDY signals for hold back flow control. Additionally, Black describes using fairness tokens (Black, col. 7, lines 36-45, col. 17, lines 26-42, col. 49, line 26-33), camp lists (Black, col. 21, lines 47-67, col. 37, line 60 through col. 39, line 26), scoreboards (Black, col. 31, line 15 through col. 35, line 58), and wall clocks (Black, col. 38, lines 40-57) to determine routing.

Thus, Black does not disclose the aforestated specifications of amended claim 9.

Accordingly, claim 9 is allowable, as are dependent claims 10, 12, 14, 27-29, and 32.

Claim 15 has been amended to specify, in part, "at least one multiplexer configured to route data to the at least one data loop output, in accordance with the at least one signal, directly from the at least one data loop input or from the at least on disk device."
In rejecting prior claim 15, the Office action points to Black at Figs. 3 and 4, col. 1, lines 14-17, col. 13, lines 33-42, col. 14, lines 9-22, and col. 15, lines 52-61. The content of the cited sections is discussed above in regard to claim 1. Thus, Black does not disclose "at least one multiplexer configured to route data to the at least one data loop output, in accordance with the at least one signal, directly from the at least one data loop input or from the at least on disk device," as specified by amended claim 15.

Accordingly, claim 15 is allowable, as are dependent claims 16-18, and 24-25.

Claim 33 has been amended to specify, "at least one processor configured to process data, including frame data, associated with the data loop." Support for the amendment may be found, for example, at Fig. 10 and p. 24, lines 26-33 of the application as filed. In rejecting prior claim 33, the Office action points to Black at Figs. 3, 7, col. 13, lines 33-42, col. 14, lines 9-22, col. 15, lines 52-61, col. 27, lines 22-35, and col. 34, lines 31-49. The content of the cited sections is discussed above in regard to claim 1. Black does not disclose "at least one processor configured to process data, including frame data, associated with the data loop," as specified by claim 33. Accordingly, claim 33 is allowable, as are dependent claims 34-36.

Dependent claims 37, 38, and 39 are new. Support for claim 37 may be found, for example, p. 16, lines 20-32. Support for claim 38 may be found, for example, at p.9, lines 19-25, and p. 14, line 19-27 of the application as filed. Support for claim 39 may be found, for example, p. 14, lines 6-9.

In view of the foregoing, the application is believed in condition for allowance, and allowance of the same is respectfully requested.

Respectfully submitted,

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